



奈米科技創新教育資源之研發與推廣中心



種子教師研習營

前瞻奈米製程－樂高奈米建築師

1.減法與加法



2.光與影的生產術－奈米微影製程

微奈米科技研究中心

林俊宏、鍾崇仁

1-28-2016



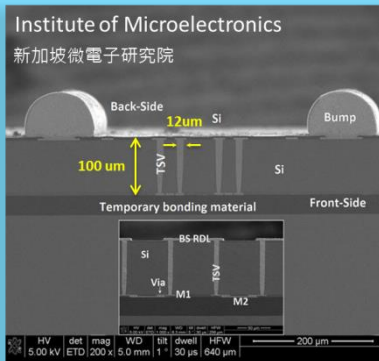
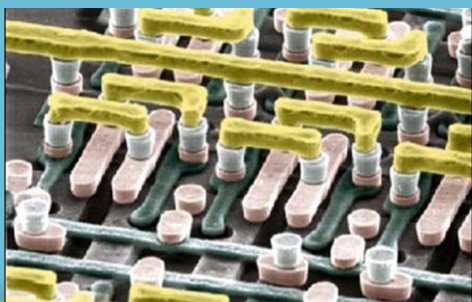
前瞻奈米製程－樂高奈米建築師

林俊宏、鍾崇仁

製深、複雜之半導體製程技術

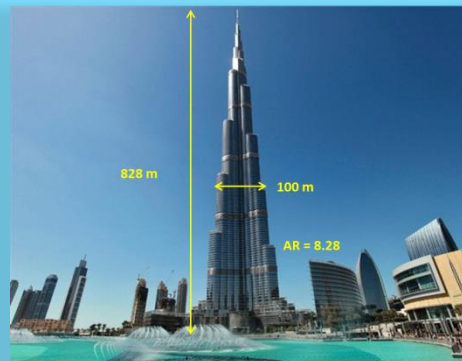
3D-IC 矽穿孔離子蝕刻製程

- 離子蝕刻機制
- 蝕刻率
- 深寬比
- 蝕刻選擇比



奈米半導體製程

- 奈米微影
- 奈米蝕刻
- 介電材料
- 電路連結



建造大樓

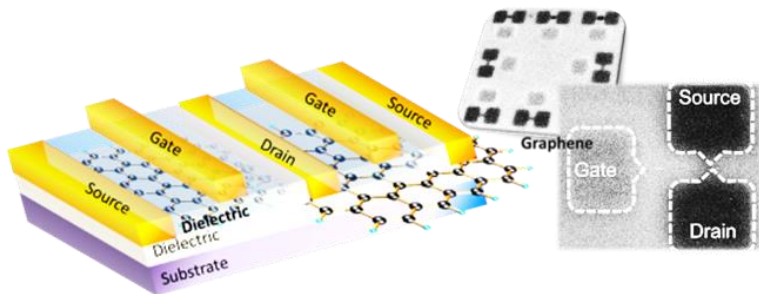
- 地基
- 鋼筋水泥
- 管道
- 動手做半導體製程樂高

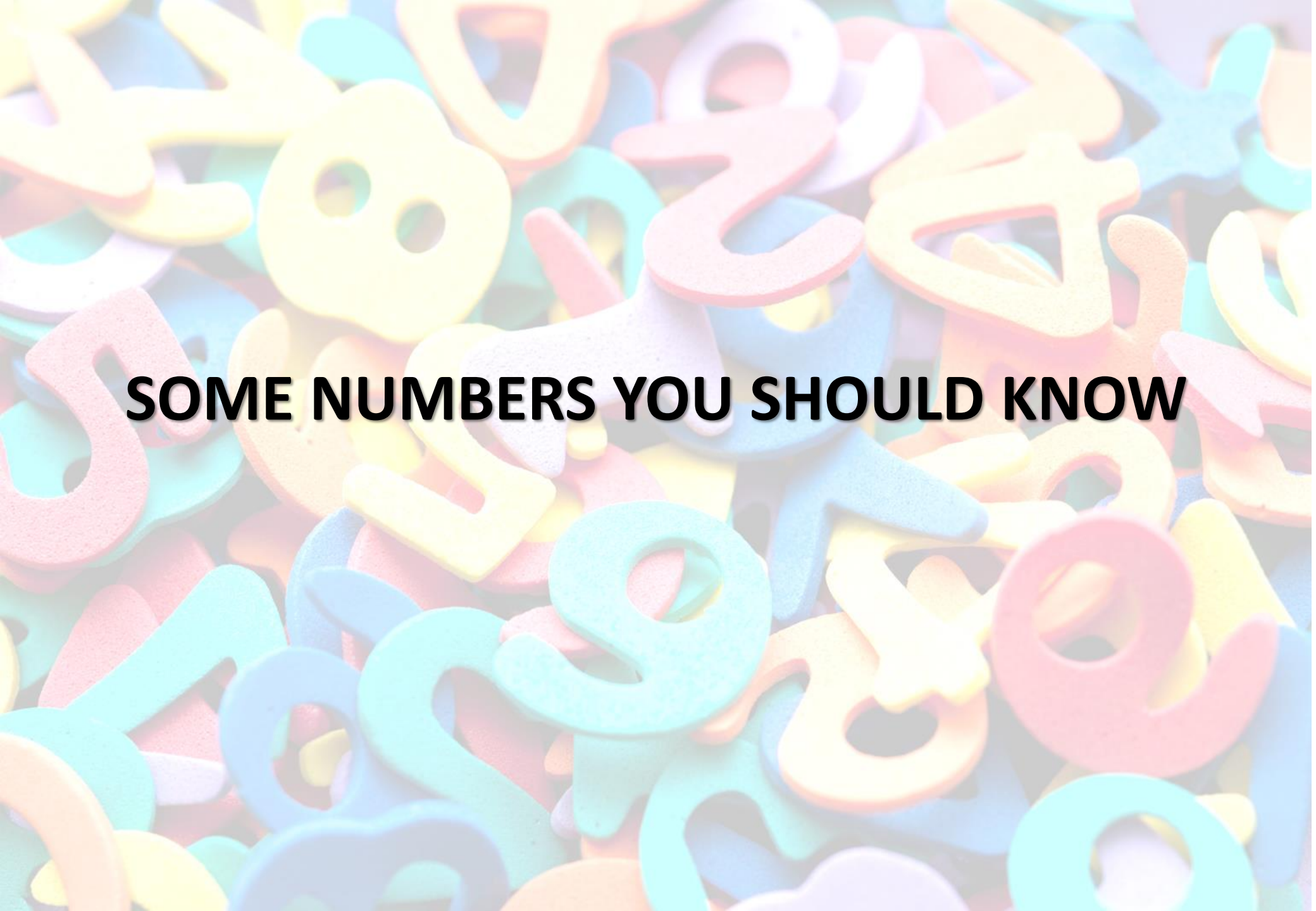
杜拜哈里發塔

- Top-down vs bottom-up
- 深寬比概念
- Bosch製程樂高演繹
- 動手做3D-IC樂高



生活化、實體化、e 化之創新教具





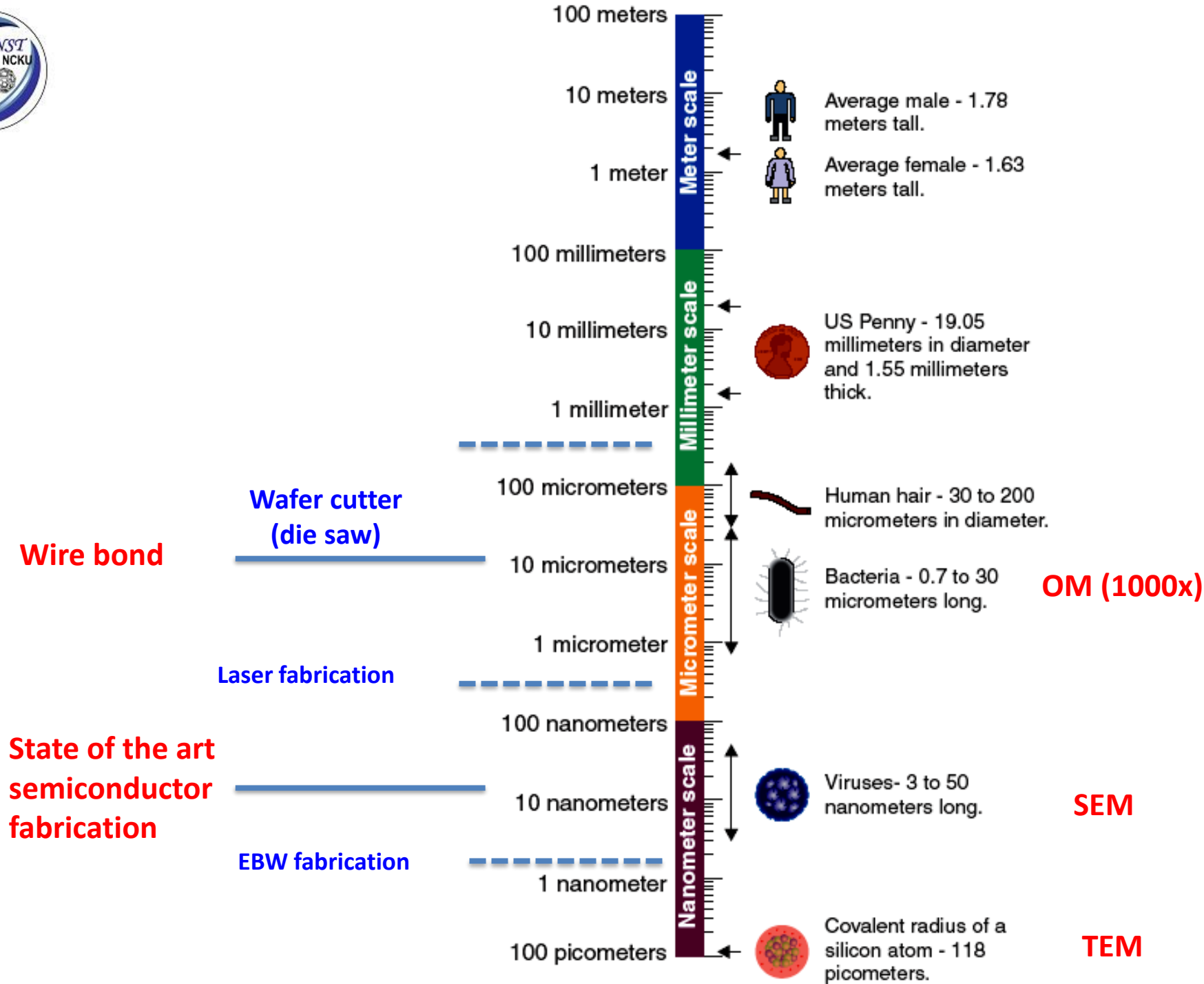
SOME NUMBERS YOU SHOULD KNOW



FABRICATION ABILITIES

OBSERVATION LIMITATIONS





OM (1000x)

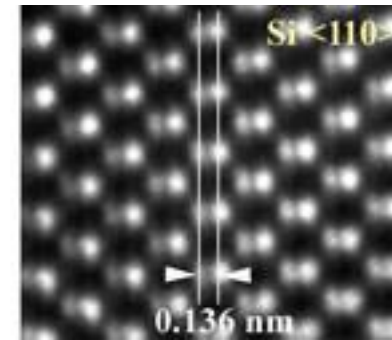
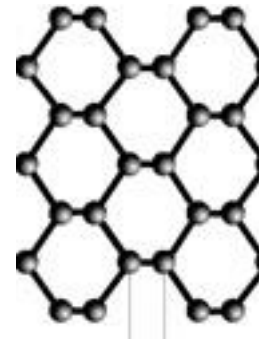
SEM

TEM

TEM, FEI Titan

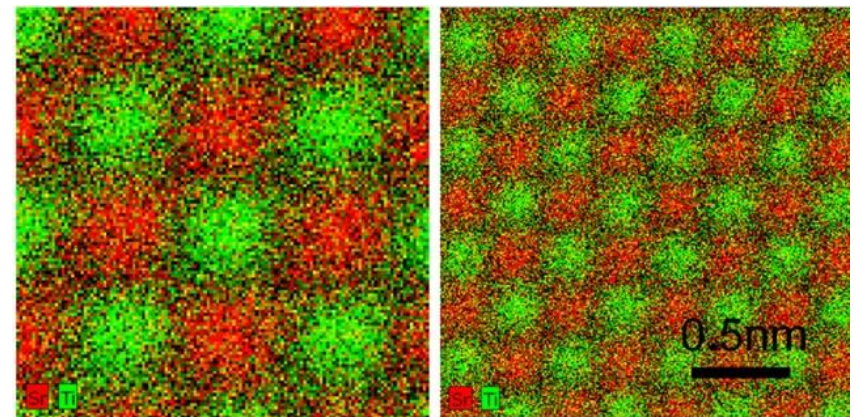


Silicon Dumbbells



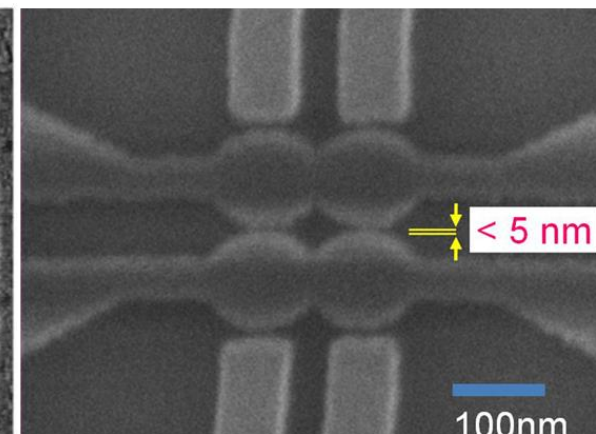
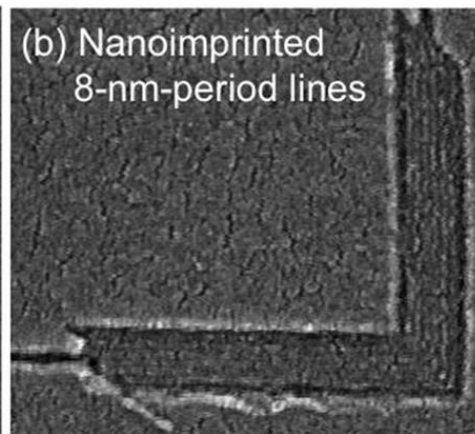
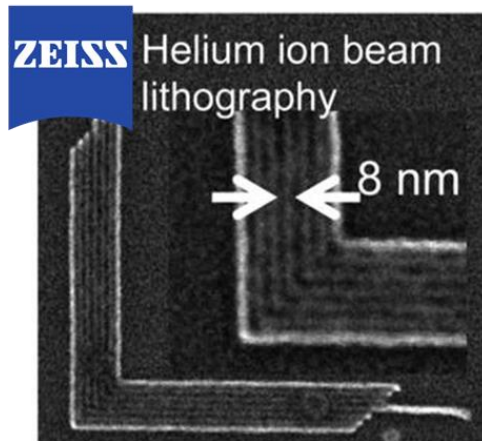
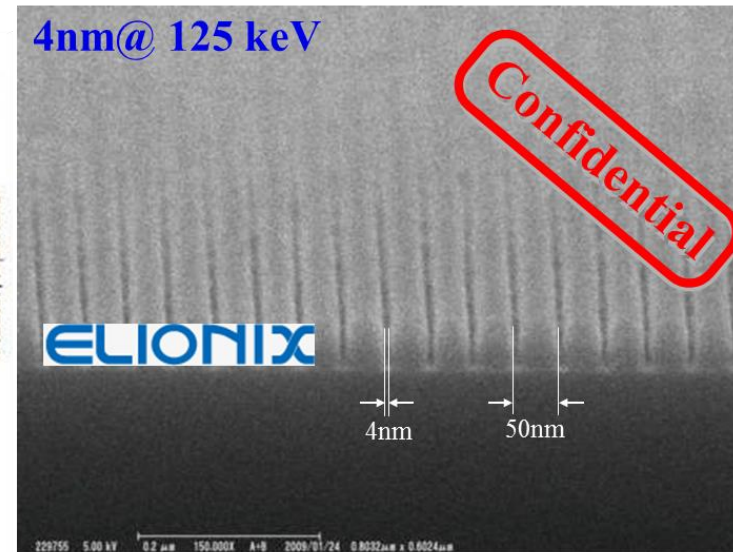
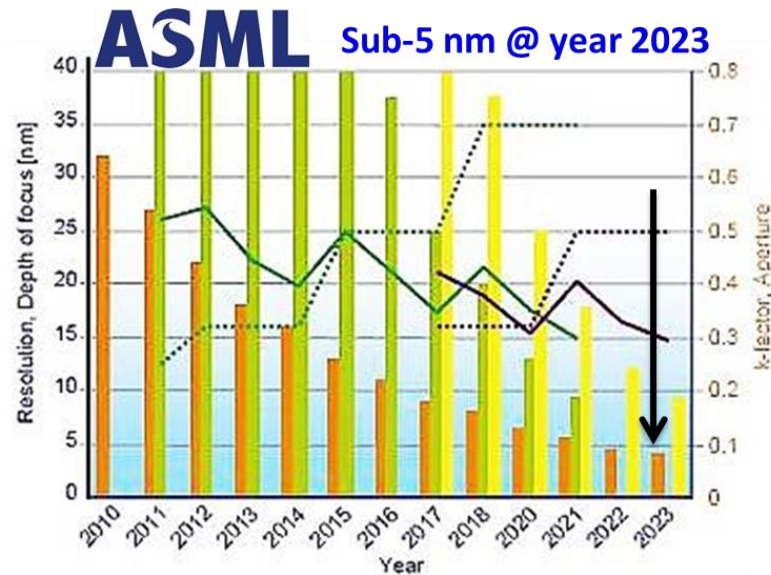
The University of Arkansas

0.075 Angstroms per pixel (EDS)



FEI

State-of-the-art Fabrication



Hiroshi Mizuta et. al., Ultrafine graphene nanodevice fabrication, 2013



RULES OF FABRICATION



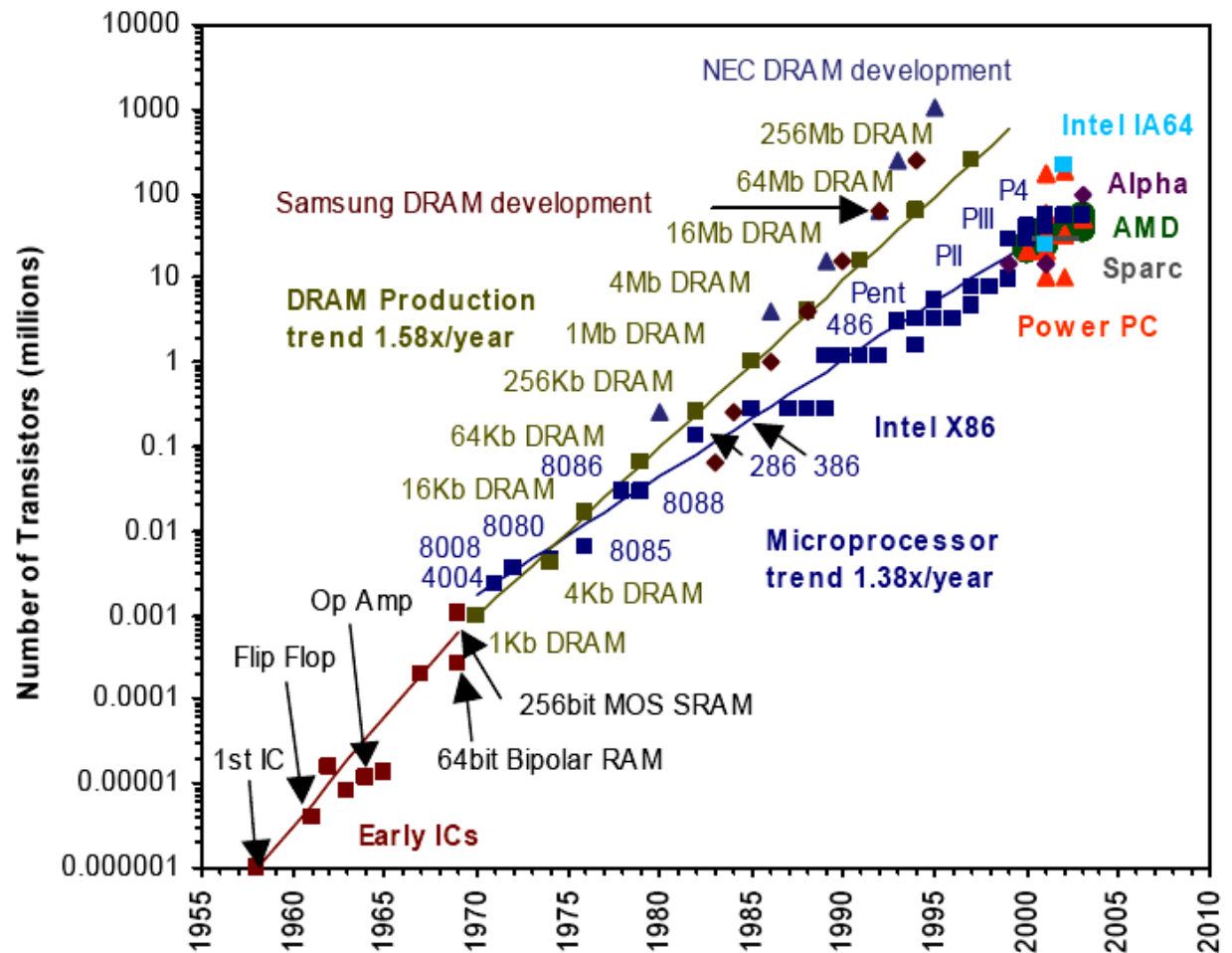
Moore's Law

- Intel co-founder **Gordon Moore** notices in 1964
 - Number of transistors doubled every 12 months
 - Slowed down in the 1980s to every 18 months
 - Amazingly still correct likely to keep until 2010

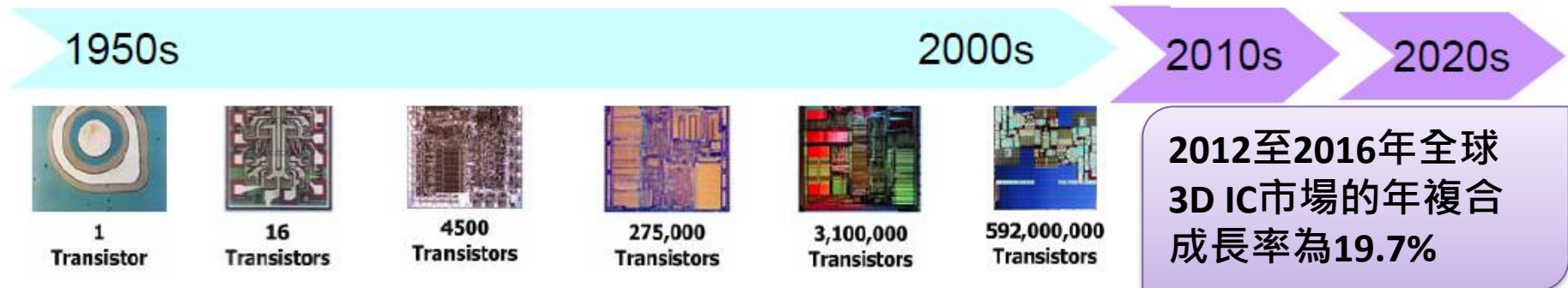
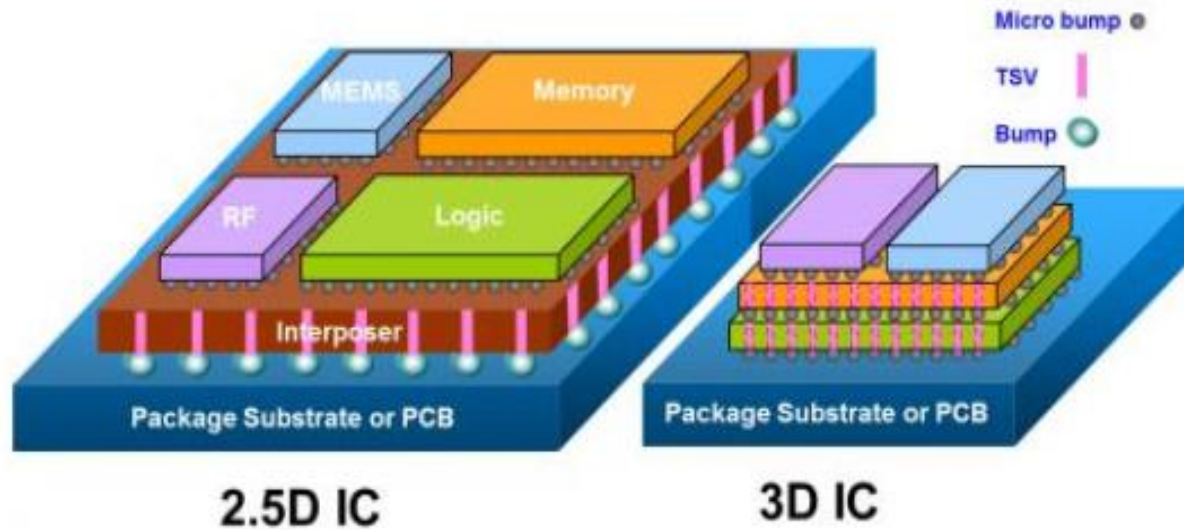


Gordon Moore
Intel Co-Founder and
Chairmain Emeritus

With Moore's Law, IC products can reach low costs, improve performance, and increase the functions.



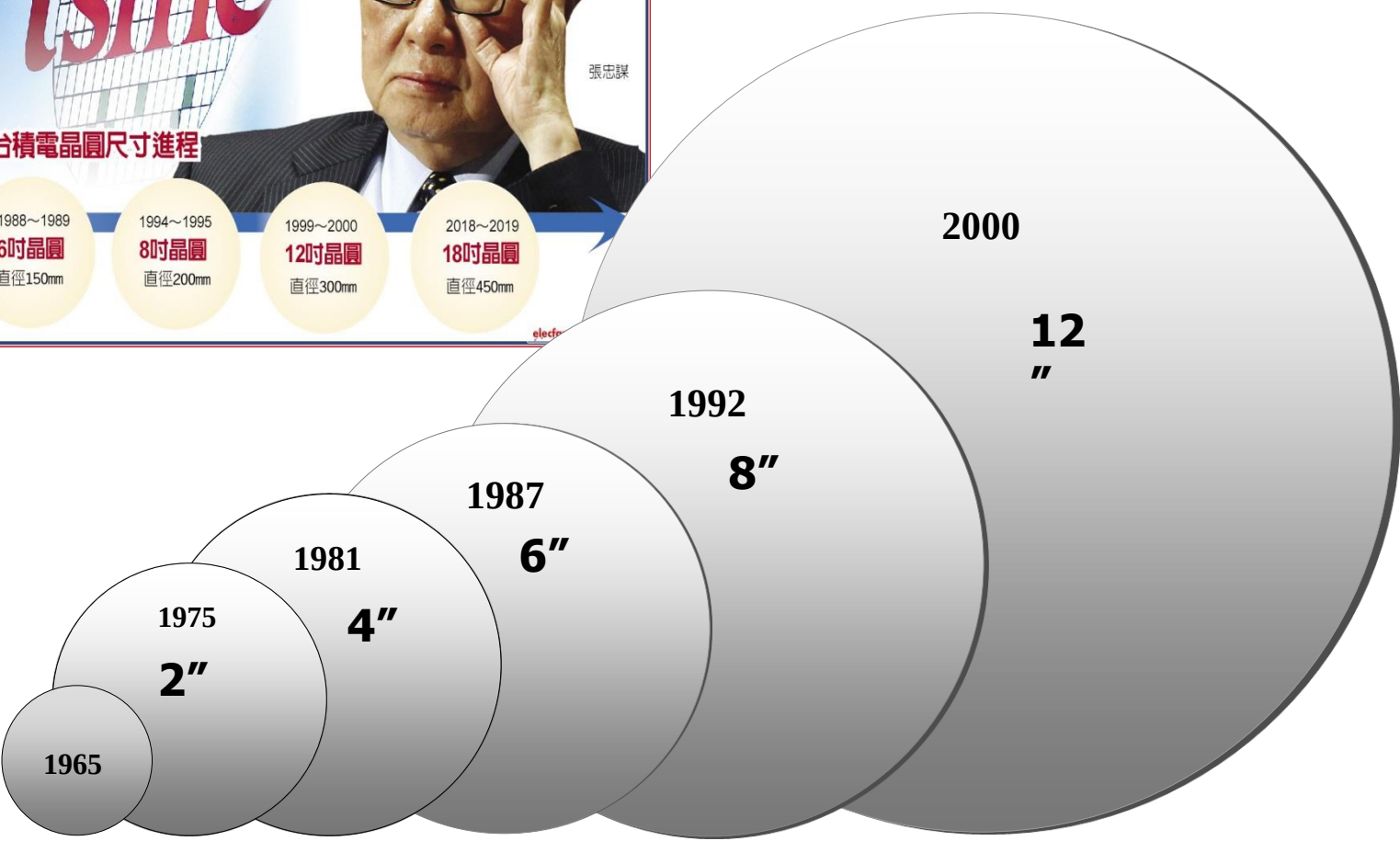
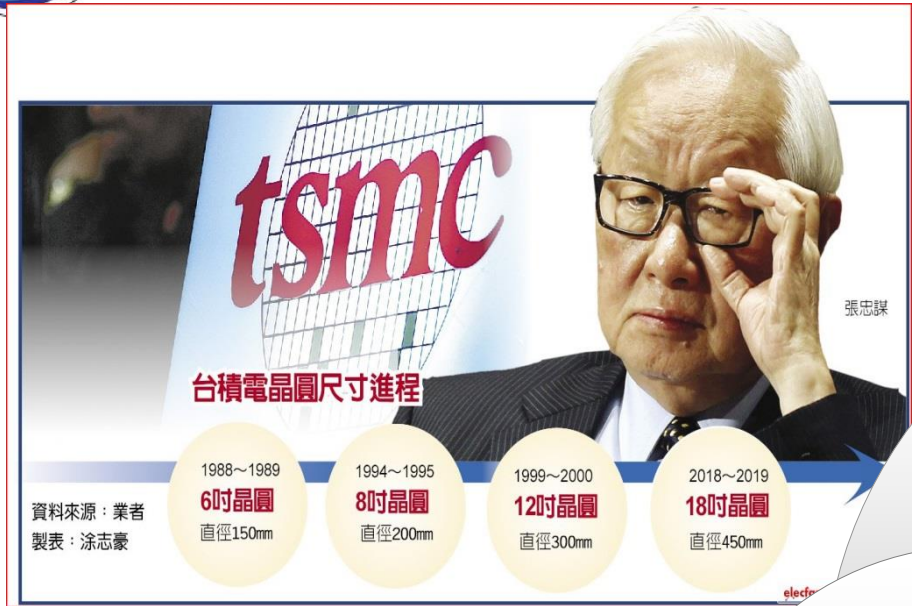
“More-than-Moore” (MtM)





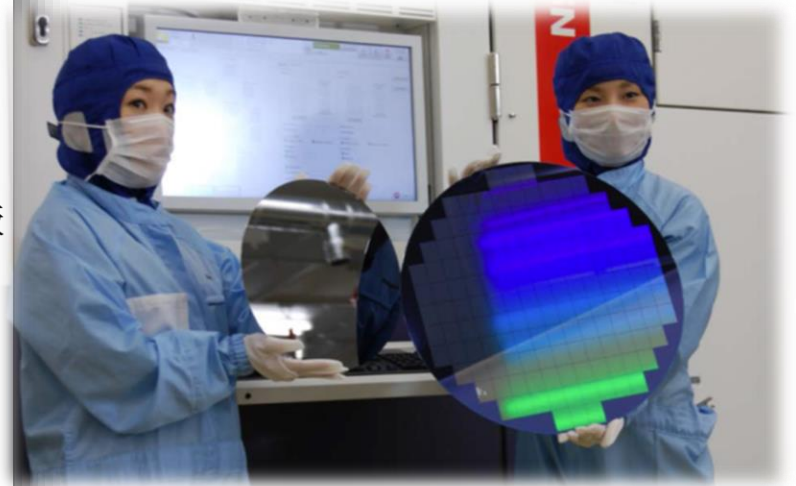
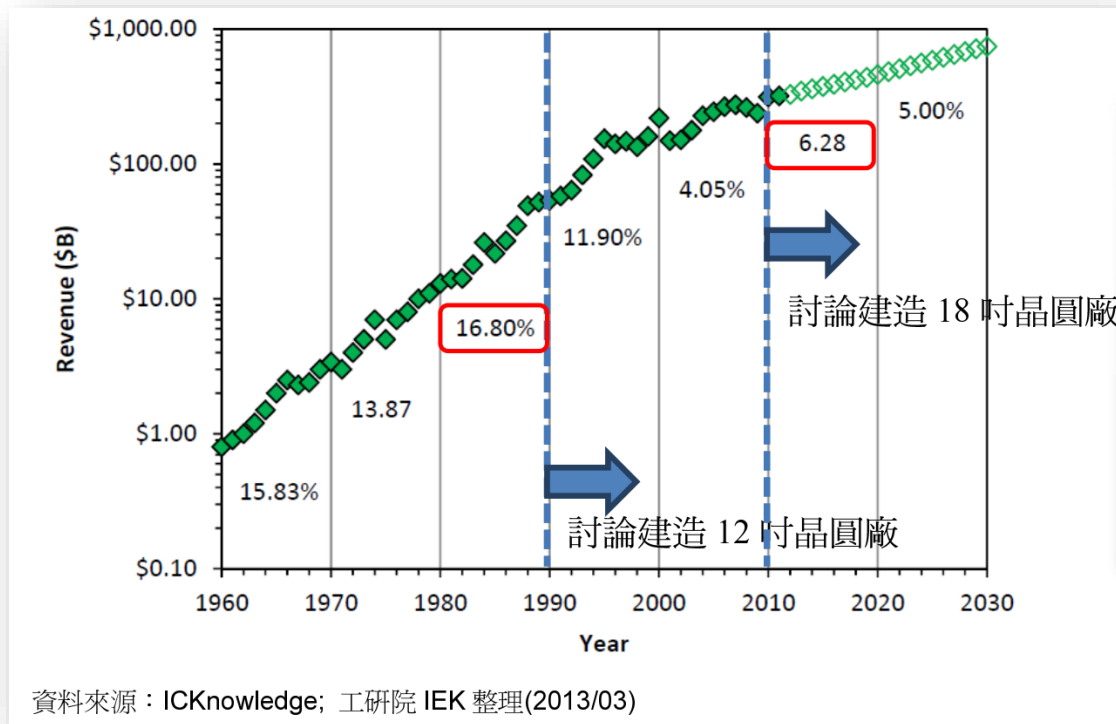
SI WAFER SIZE?
GLASS SUBSTRATE SIZE?

Evolution of Wafer Size



G450 Generation

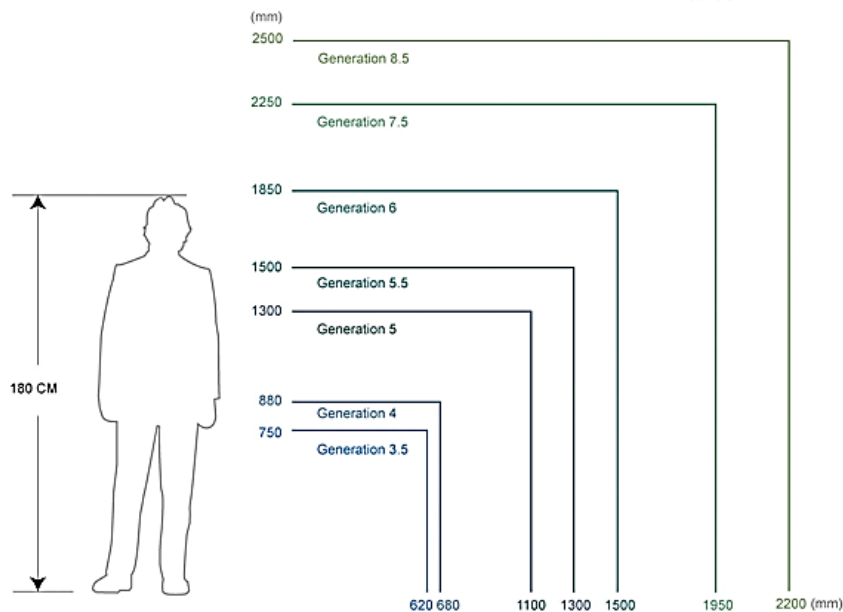
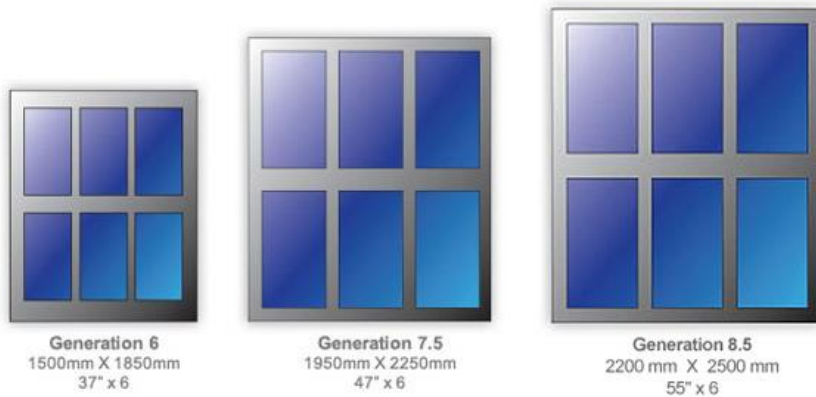
張忠謀：中科新廠6月動土 2016中完工



Source: G450C, 2014

8 吋製程轉往 12 吋製程時，半導體成長約有 17%成長率，預估12 吋轉往 18 吋時約只有 4~6%的成長

Generation of Glass

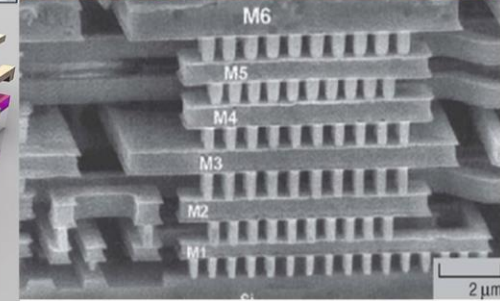
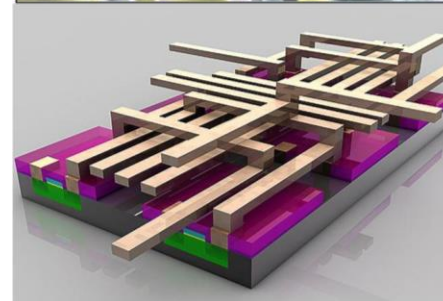
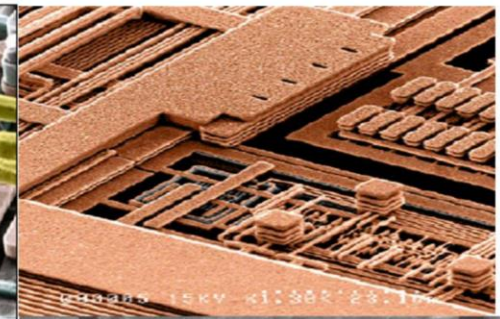
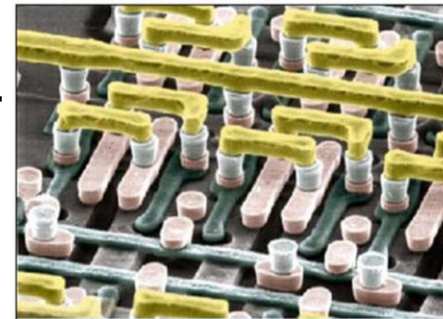
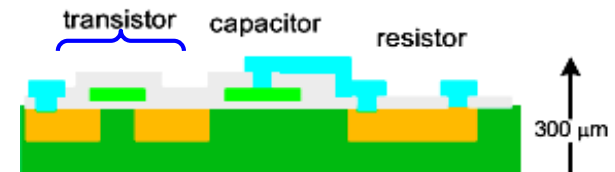
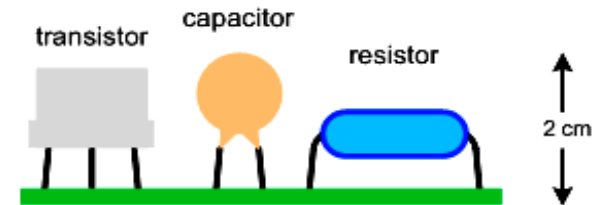
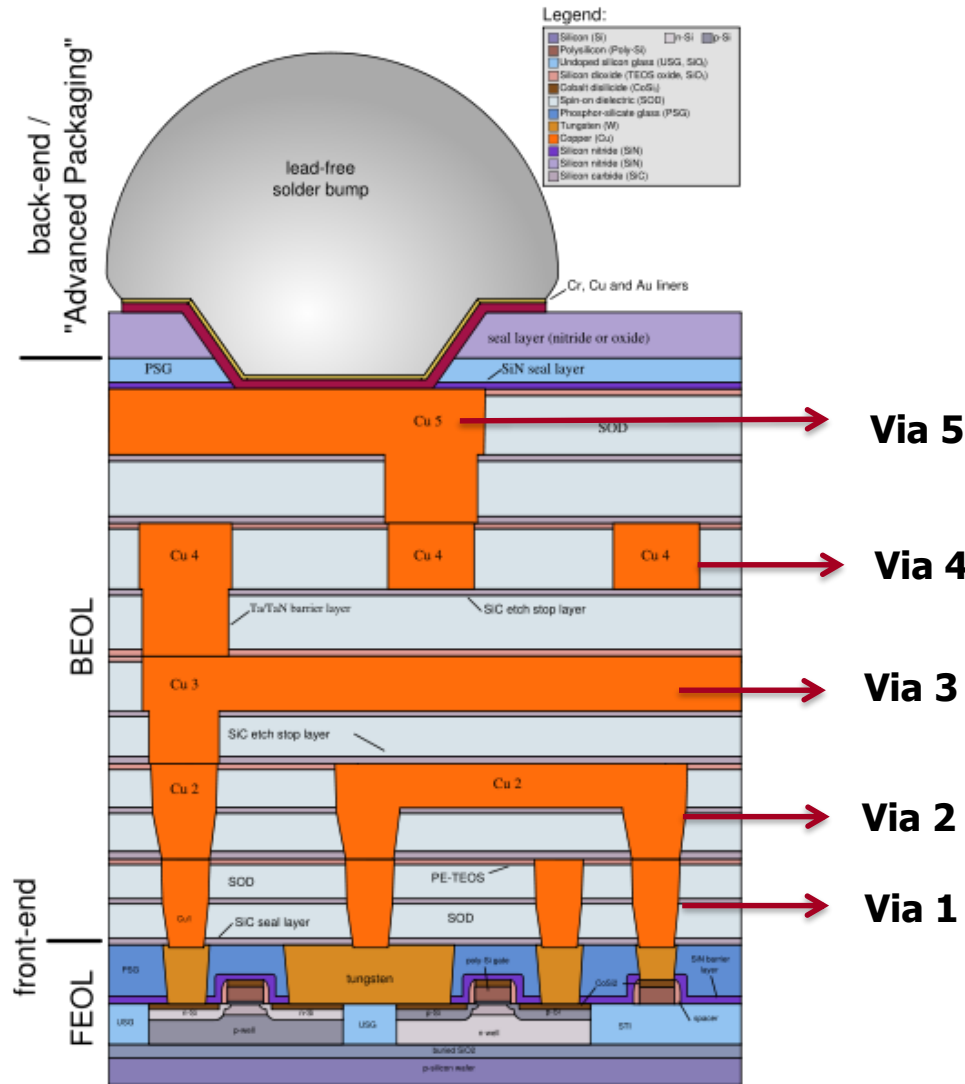




HOW MANY LAYERS?

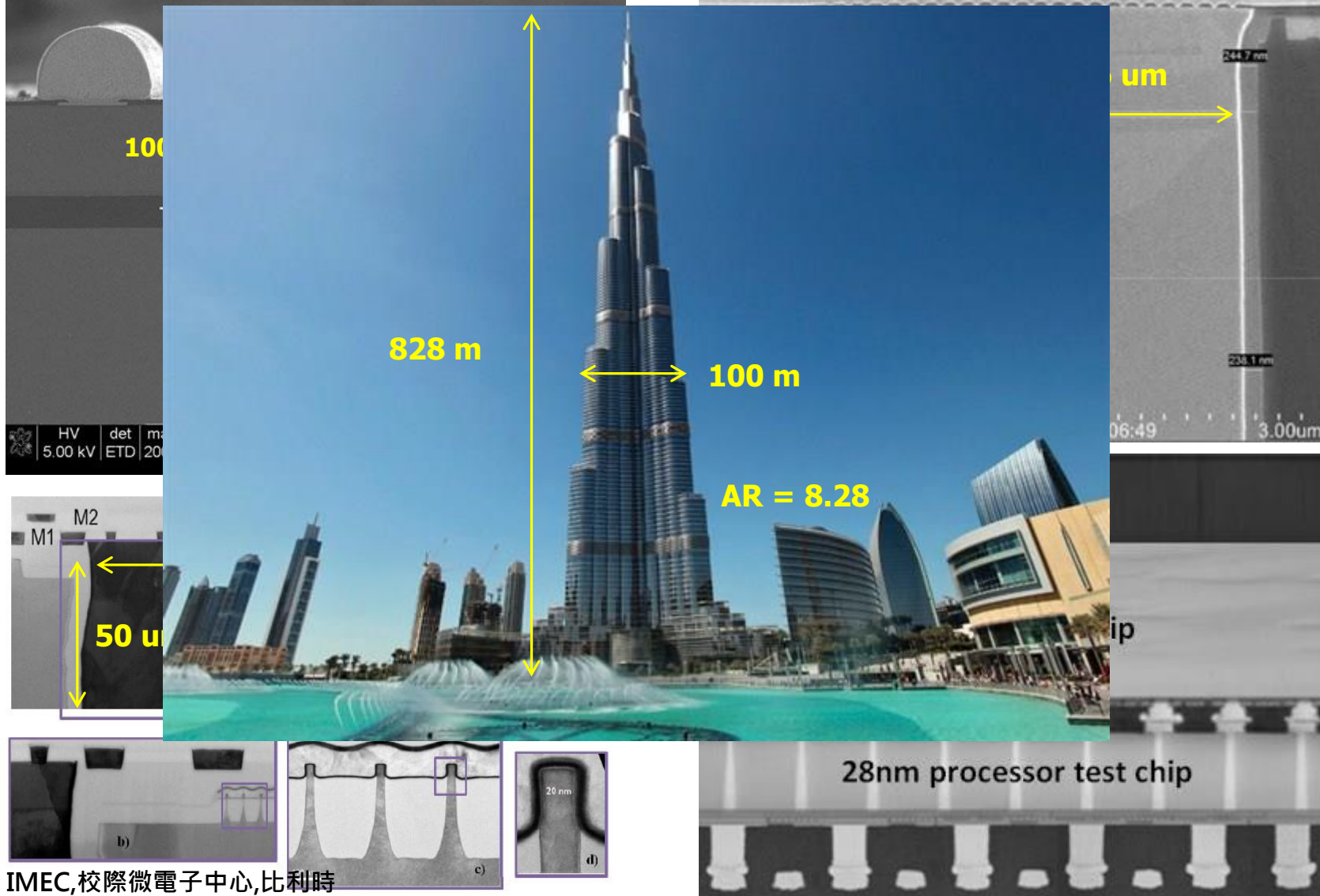
半導體製程能力之現況

12 metal layers / through-silicon via (TSV)





ASPECT RATIO?





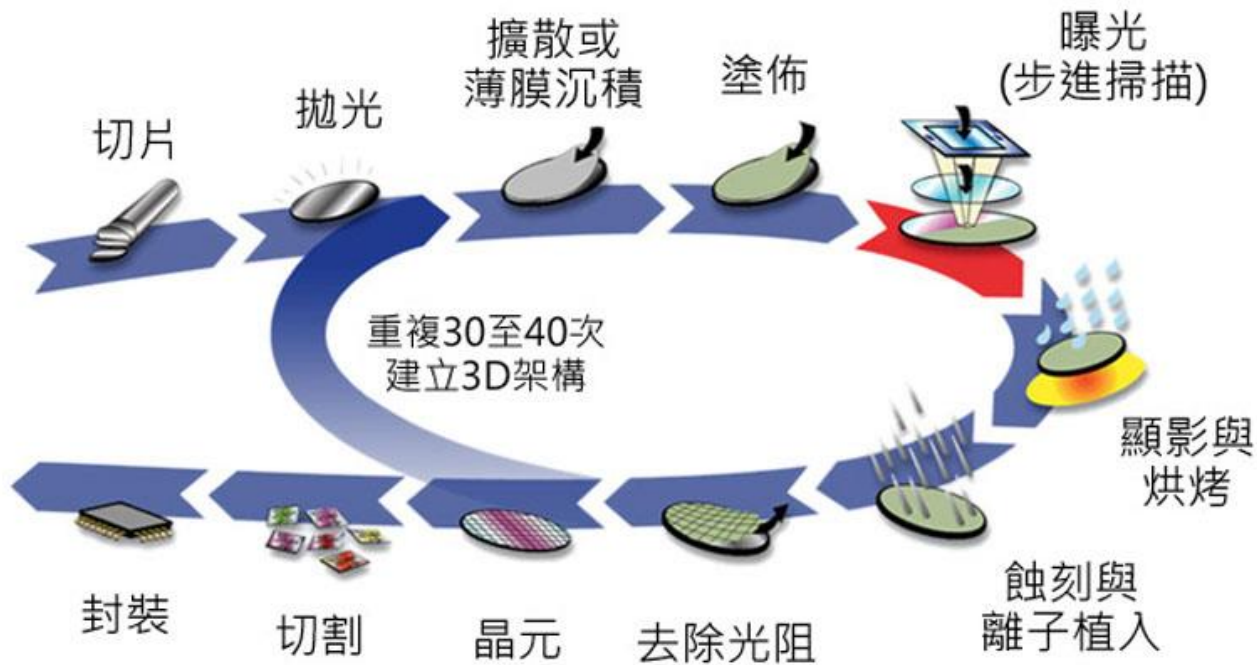
萬丈高樓平地起



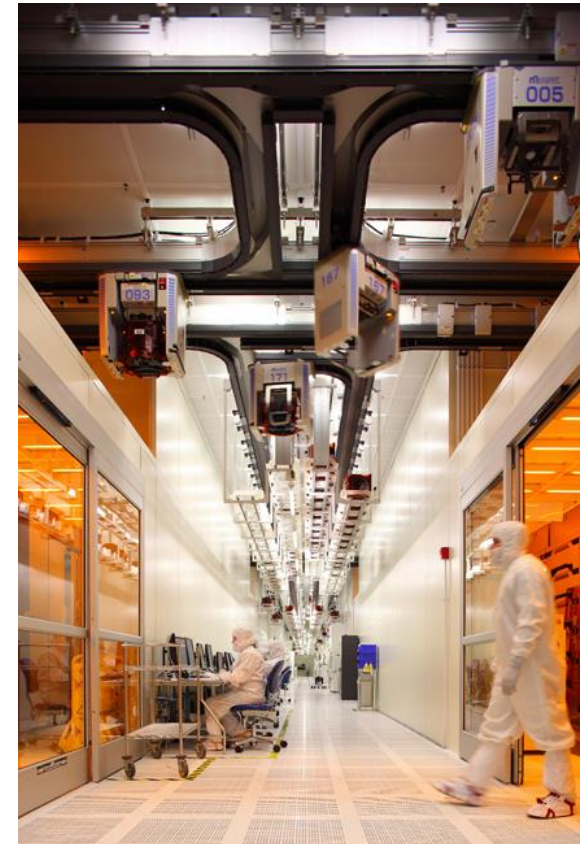
Lithography

Lithography (from Greek λίθος, *lithos*, "stone" and γράφειν, *graphein*, "to write")

Semiconductor Device Fabrication Processes

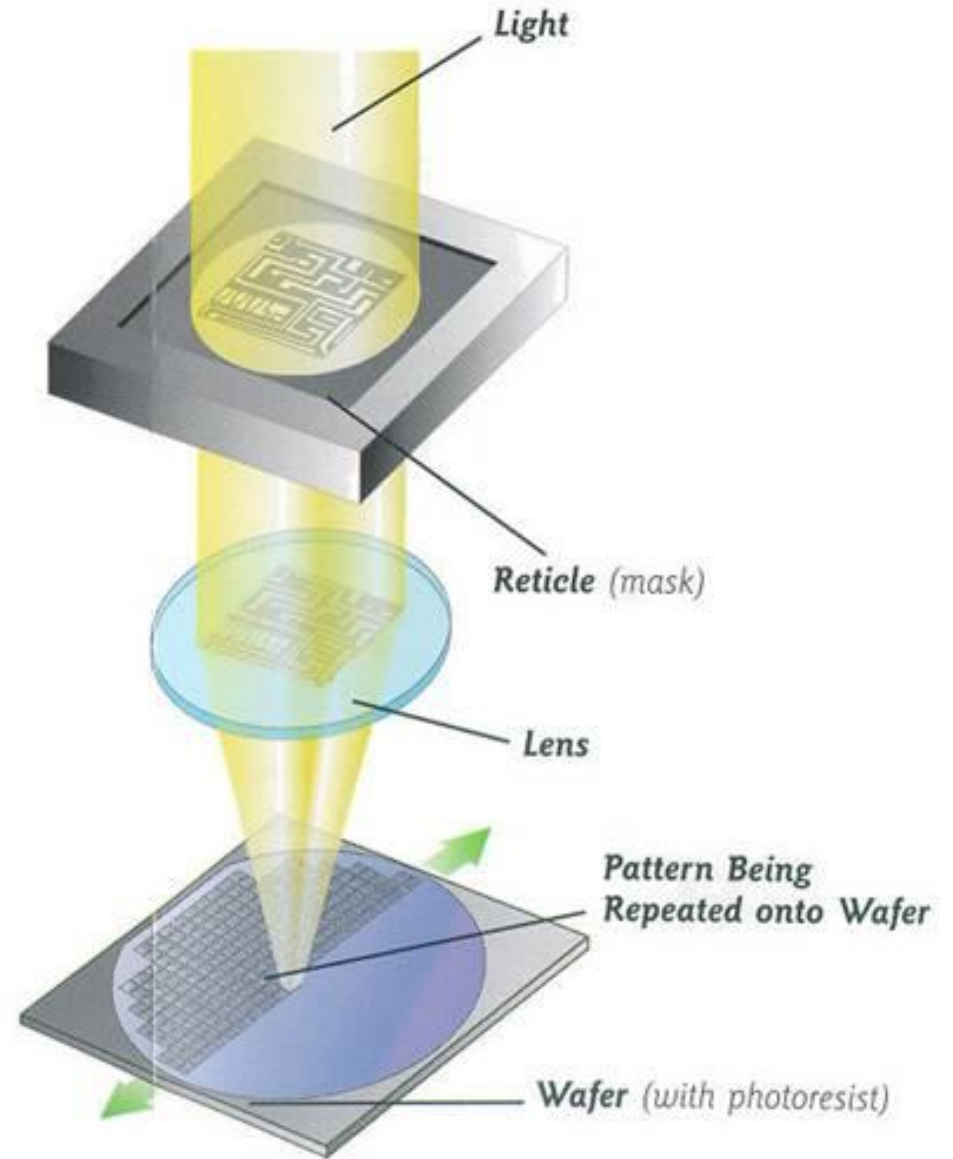
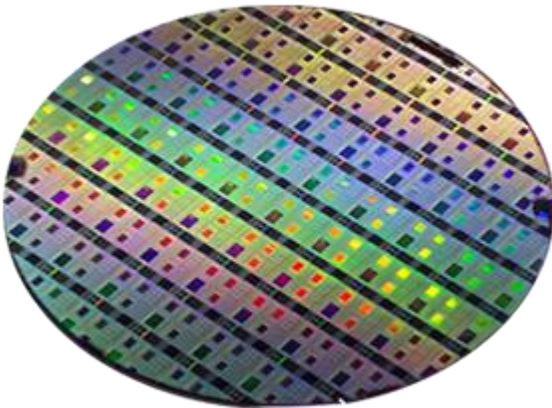
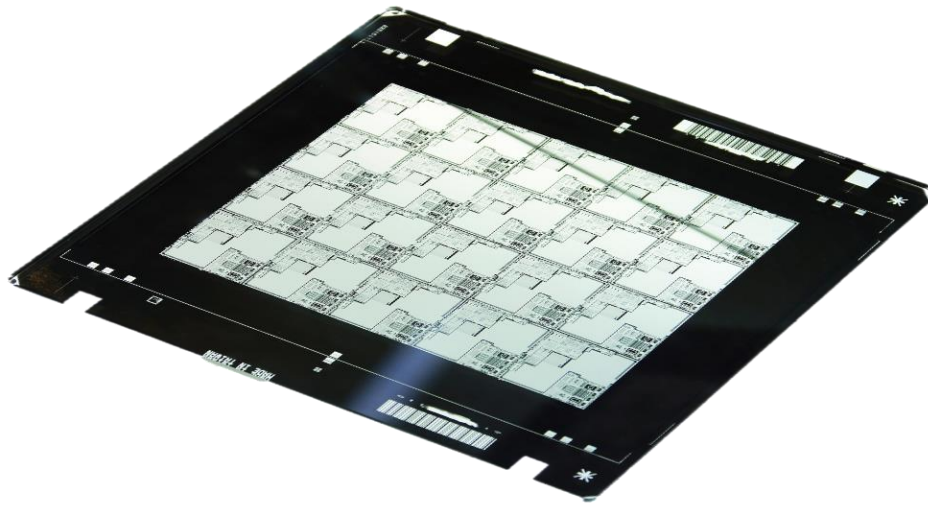


Intel-Micron



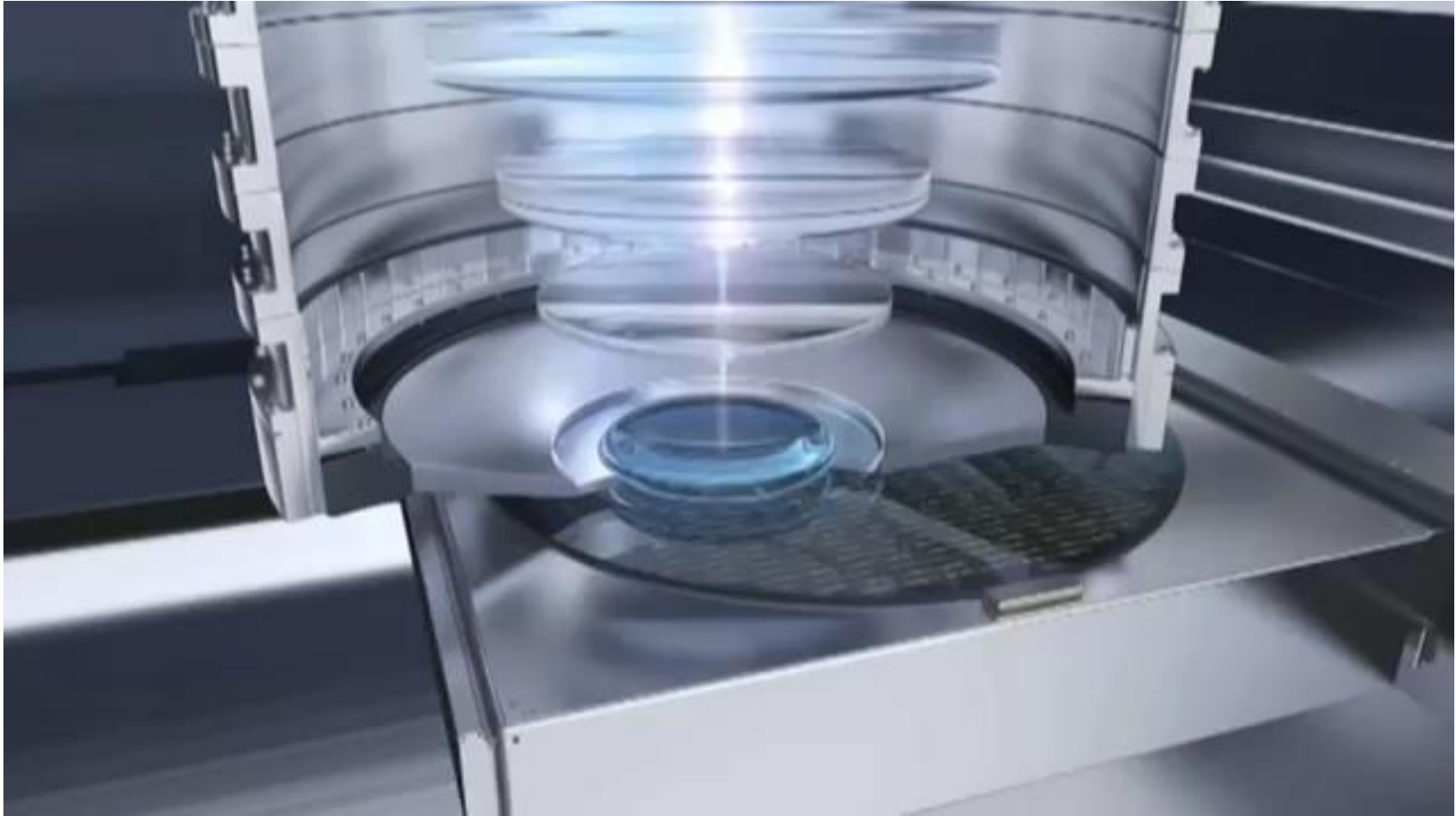
<http://goo.gl/8HrPI8>

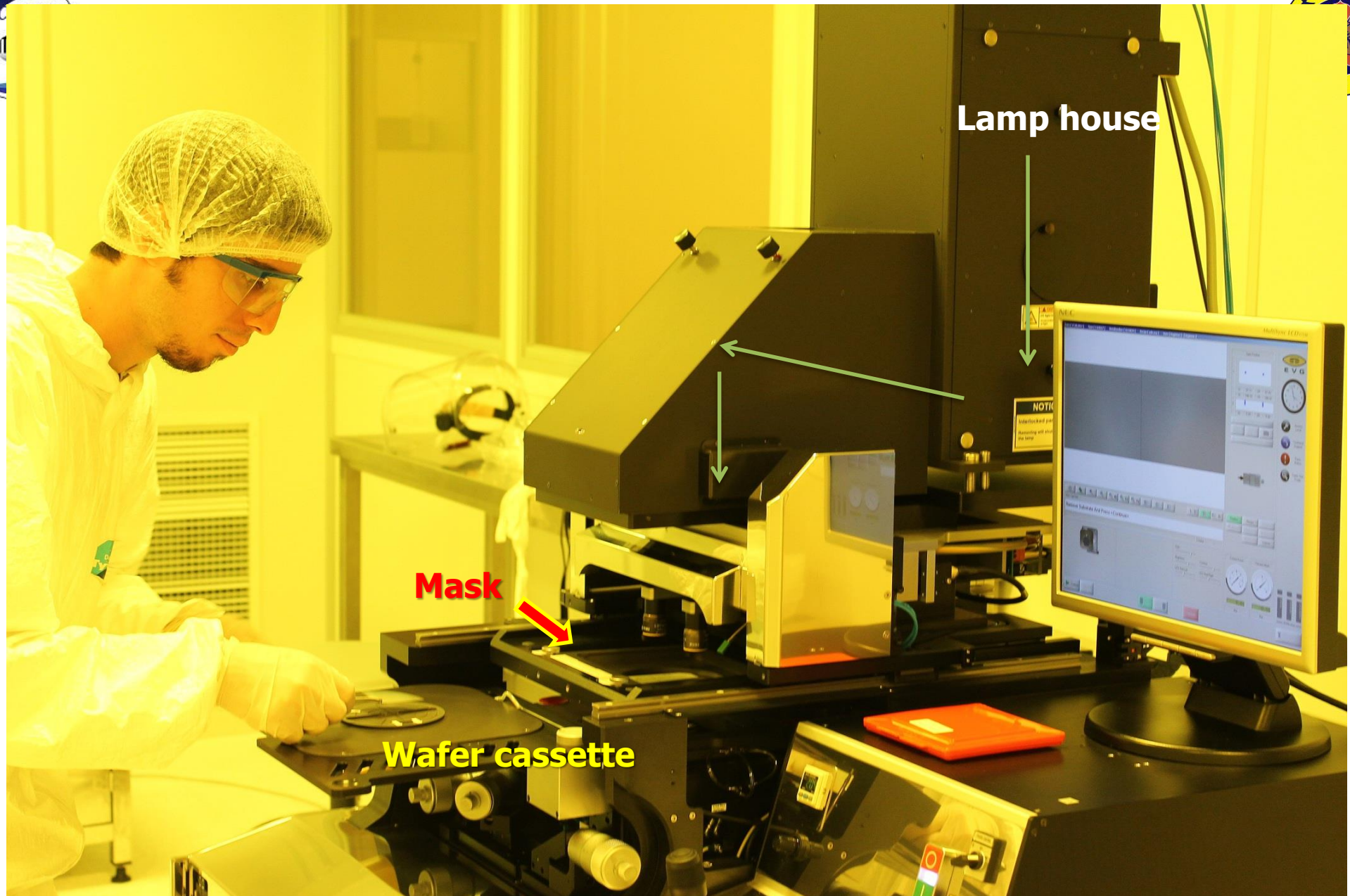
微影



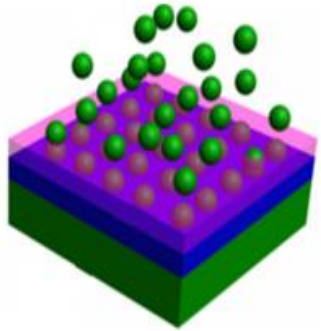


How water can help?



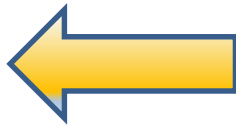
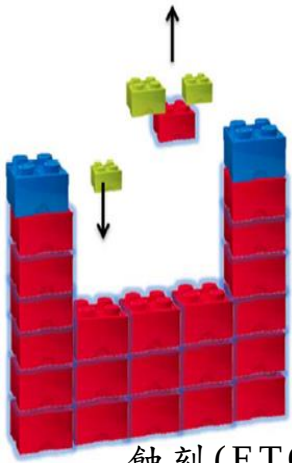
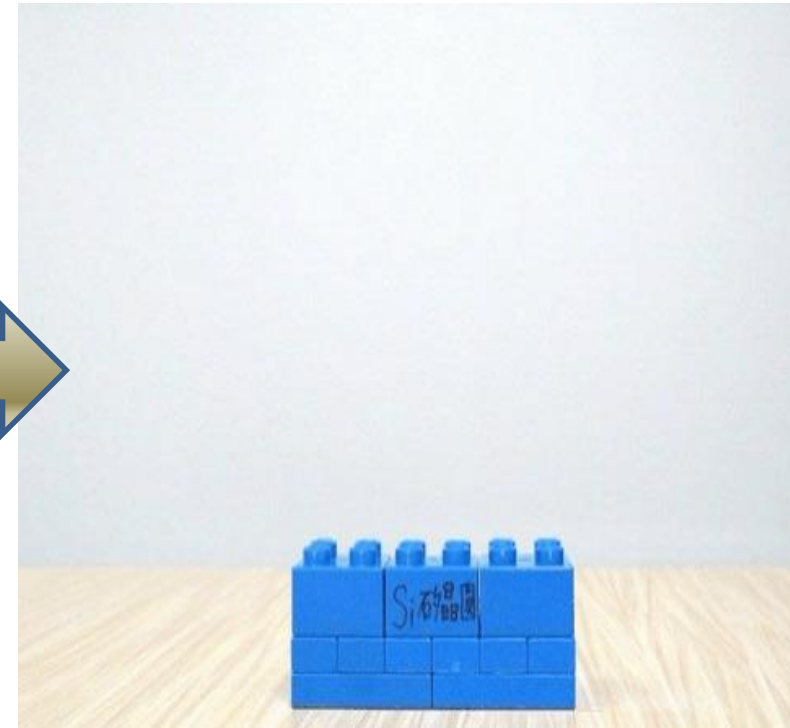
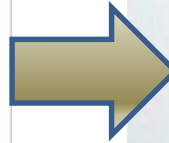
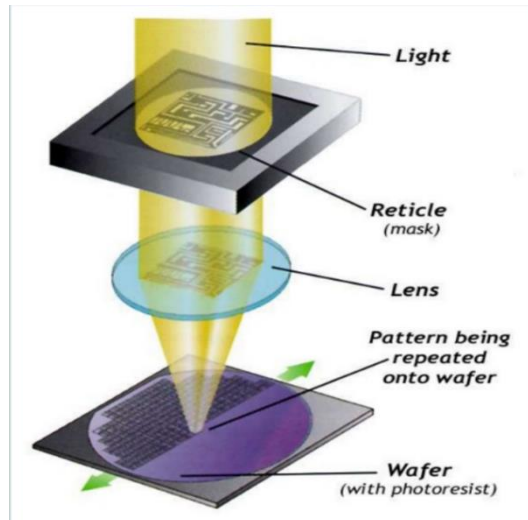


減法與加法



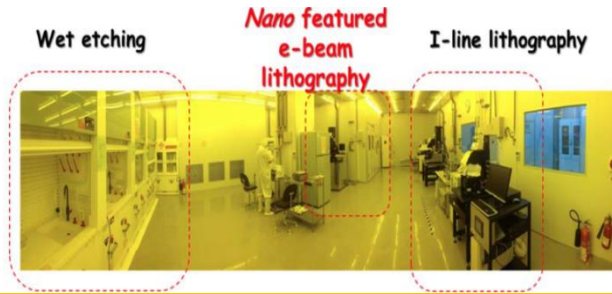
微影製程
(PHOTOLITHOGRAPHY)：
利用光學技術，將所需設計轉
印於薄膜上

薄膜沉積：藉由化學或物理
的方法(CVD /pvd)，將所需
材料層，沉積於矽晶圓上



蝕刻(ETCHING)：用化學或物
理的方法，去除不需要的部分，
保留設計

- 微影製程必須在無塵室裡進行，首先你必須穿的像這樣
- 然後在這樣的環境下進行製程



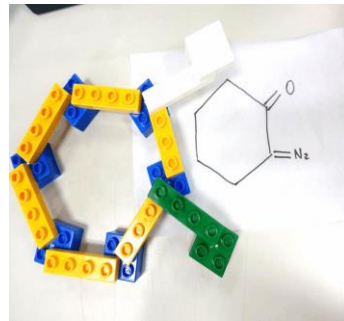
- 為了讓微影的概念更生活化，在這裡使用日光顯影實驗做說明



光阻塗佈
Coating



UV曝光
Exposure



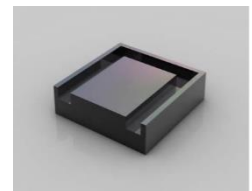
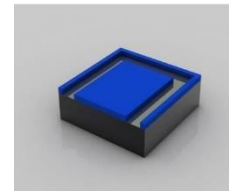
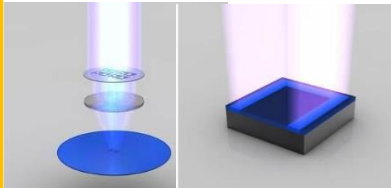
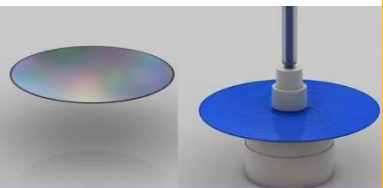
化學反應
Reaction



顯影
Develop



成像
Pattern

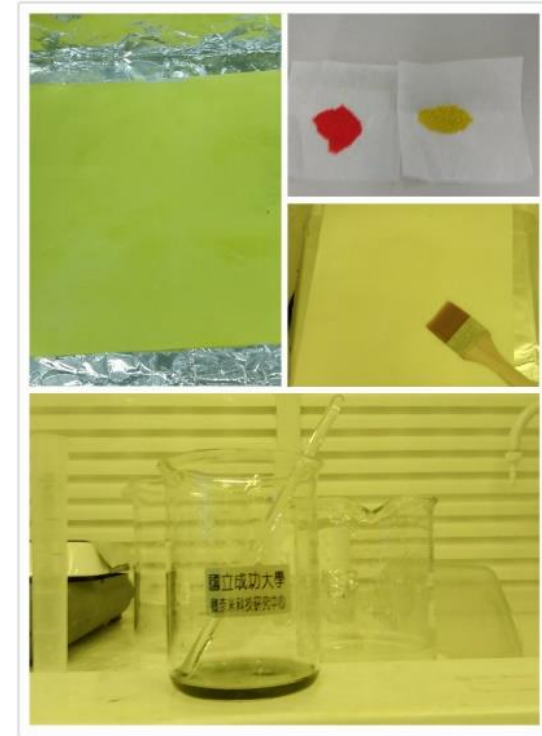


材料

- 檸檬酸鐵銨 (常溫常壓下穩定之化合物)
- 鐵氰化鉀 (常溫常壓下穩定之化合物)
- 純水
- 燒杯
- 攪拌玻棒
- pp廣口瓶
- 美術紙
- 水彩筆
- 印表機用透明膠片

實驗步驟

1. 將檸檬酸鐵銨與純水，依重量比1:4配製成溶液
2. 將鐵氰化鉀 與純水，依重量比1:10配製成溶液
3. 將兩溶液等比例混合於PP瓶中，即為感光液(概念：光阻)
4. 取透明膠片製作曝光用 光罩
5. 取美術紙塗佈感光液後，進行日光曝曬，最後以清水泡洗得到預期圖案(概念：微影製程：塗佈Coating → 曝光Exposure → 顯影Development)



正光阻：顯影後圖形與光罩相同

負光阻：顯影後圖形與光罩互補(本計畫示範)



THANKS

前瞻微奈米科技研究 + 核心設施企業化經營

成功大學微奈米科技研究中心